Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	((grading adj rate) and Ge and "%" and (epitaxially or epitaxial) and threading and dislocation).clm.	US-PGPUB; USPAT	OR	ON	2005/07/26 15:04
L2	1	((grading adj rate) and Ge and (epitaxially or epitaxial) and threading and dislocation).clm.	US-PGPUB; USPAT	OR	ON	2005/07/26 15:05
L3	1118	438/37,44,46,87.ccls.	US-PGPUB; USPAT	OR	ON	2005/07/26 15:10
L4	257	3 and Ge	US-PGPUB; USPAT	OR	ON	2005/07/26 15:08
L5	153	4 and (Si with Ge)	US-PGPUB; USPAT	OR	ON	2005/07/26 15:10
L6	113	5 and @ad<"20020823"	US-PGPUB; USPAT	OR	ON	2005/07/26 15:10
L7	953	257/18,19,191,616.ccls.	US-PGPUB; USPAT	OR	ON	2005/07/26 15:10
L8	357	7 and (Si with Ge)	US-PGPUB; USPAT	OR	ON	2005/07/26 15:10
L9	241	8 and @ad<"20020823"	US-PGPUB; USPAT	OR	ON	2005/07/26 15:11
L10	236	9 not 6	US-PGPUB; USPAT	OR	ON	2005/07/26 15:11

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	270	(epitaxial or epitaxially) same ((graded or gradient or grading) with Ge)	US-PGPUB; USPAT	OR	ON	2005/07/26 13:56
L2	212	1 and @ad<"20030822"	US-PGPUB; USPAT	OR	ON	2005/07/26 13:14
L3	141	1 and @ad<"20020823"	US-PGPUB; USPAT	OR	ON	2005/07/26 13:55
L4	1	("6232138").PN.	US-PGPUB; USPAT	OR	OFF	2005/07/26 13:55
L5	22	(epitaxial or epitaxially) same ((graded or gradient or grading) with Ge)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 13:56

DOCUMENT-IDENTIFIER: US 20030052334 A1

TITLE: Structure and method for a high-speed semiconductor device

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Detail Description Paragraph - DETX (2):

[0015] FIG. 1 is a schematic of the layer structure upon which strained Ge channel MOSFETs are created. The layer structure includes a high quality strained Ge channel layer 14 provided on a virtual substrate 10. This strained Ge channel layer 14 may be provided on virtual substrate 10 either through epitaxial deposition or through wafer bonding techniques. In the exemplary embodiment shown in FIG. 1, the virtual substrate 10 includes a Si substrate 11, a graded composition SiGe layer 12, and a relaxed SiGe cap layer 13. The **graded** composition SiGe layer 12 is **graded** from approximately 0% **Ge** to a final concentration between 50% **Ge** and 95% **Ge at a grading** rate, for example, of 10% **Ge**/micron for a final thickness of approximately 5.0-9.5 microns. A method for providing high quality graded buffer layers is disclosed in U.S. Pat. No. 6,107,653 by Fitzgerald et al. The relaxed SiGe cap layer 13 contains 50% Ge to 95% Ge, for example, and has a thickness of 0.2-2.0 microns. A strained Ge channel layer 14 is provided on the virtual substrate 10. The strained Ge channel layer 14 has a thickness of 50 .ANG.-500 .ANG. and is compressively strained. The strained Ge channel layer 14 may grown at reduced temperature (T.sub.growth<550.degree. C.) to suppress strain-induced surface undulations and improve surface morphology, forming a strained Ge channel layer that is substantially planar. This planarity improves carrier mobility and facilitates device fabrication. The strained Ge channel layer 14 provides enhanced mobility and performance when it is used to create MOSFETs, while the virtual substrate 10 provides the necessary defect control and large area substrates for integrated circuit manufacturing. In a preferred embodiment, the strained Ge channel layer 14 is fabricated on the virtual substrate 10, which includes a relaxed SiGe cap layer 13 that is 70% Ge.

Detail Description Paragraph - DETX (4):

[0017] FIG. 3 is a schematic of the layer structure upon which relaxed Ge channel MOSFETs are created. The layer structure includes a high quality relaxed Ge layer 34 provided on a virtual substrate 30. This relaxed Ge layer 34 may be provided on the virtual substrate 30 either through epitaxial deposition or through wafer bonding techniques. In the exemplary embodiment

shown in FIG. 3, the virtual substrate includes a Si substrate 31 and a graded composition SiGe layer 32. The **graded** composition layer 32 is **graded** to a final **Ge** percentage of approximately 100% at a **grading** rate, for example, of 10% Ge/micron for a final thickness of approximately 10 microns. The relaxed Ge channel layer 34 may have a thickness of 50 .ANG.-2 microns.

US-PAT-NO: 6680495

DOCUMENT-IDENTIFIER: US 6680495 B2
See image for Certificate of Correction

TITLE: Silicon wafer with embedded optoelectronic material for monolithic OEIC

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Detailed Description Text - DETX (4):
The combination of graded layer growth and wafer bonding removes these two problems and provides tremendous flexibility to create new integrated semiconductor platforms on Si substrates. Consider again the example of bonding **Ge** to Si, this time using the **graded** layer/wafer bonding technique illustrated in FIGS. 1A-1D. In this technique, a **graded** SiGe layer 102 (**graded** from 0-100% **Ge) is epitaxially** grown on a Si substrate 100 of any diameter. A **Ge** layer 104 is then grown on the SiGe **graded** layer 102. In order to reduce surface roughness, a planarization step such as chemical mechanical polishing can be inserted during growth of the SiGe graded layer 102, as described in U.S. Pat. No. 6,107,653, incorporated herein by reference. Also note that any of the layers described in this invention can receive planarization steps, if desired.

Detailed Description Text - DETX (6):
Once the wafers are bonded, the original Si substrate 100 can then be ground and selectively etched back. In one embodiment (shown in FIG. 1C), the SiGe **graded** layer 102 can also be completely removed to leave only the **Ge** layer 104 on the new host Si substrate 106. A Si cap layer 108 can now be epitaxially grown on top of this structure, such that the optically-active layer 104 (Ge in this case) is effectively embedded in a Si wafer as shown in FIG. 1D.

Detailed Description Text - DETX (16):
As another example, through compositional grading of SiGe and InGaAs layers on Si, it is possible to create a bonded layer of InP or InGaAs on Si as well. This can be accomplished as follows. First, a **graded** SiGe epitaxial layer (**graded** from 0-100% **Ge) is epitaxially** grown on a Si substrate. Since GaAs and Ge have nearly equal lattice constants, a GaAs layer can then be epitaxially grown on top of the Ge layer. At this point, the GaAs layer can be wafer bonded to another Si substrate such that the embedded active optoelectronic

layer was GaAs. Alternatively, a relaxed, graded InGaAs layer can be grown on the GaAs layer, graded from 0% In to some desired In concentration, as described in U.S. Pat. No. 6,232,138, incorporated herein by reference. The InGaAs layer can be wafer bonded to another Si substrate.

US-PAT-NO: 6525338

DOCUMENT-IDENTIFIER: US 6525338 B2

TITLE: Semiconductor substrate, field effect transistor, method of forming SiGe layer and method of forming strained Si layer using same, and method of manufacturing field effect transistor

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Brief Summary Text - BSTX (14):

Furthermore, a SiGe layer formation method according to the present invention is a method of forming a SiGe layer on top of a Si substrate, wherein a step for epitaxially growing a SiGe **gradient** composition layer in which the **Ge** composition ratio gradually increases from the **Ge** composition ratio of the base material, and a step for epitaxially growing, on top of the SiGe **gradient** composition layer, a SiGe constant composition layer in which the **Ge** composition ratio is the same as that of the final **Ge** composition ratio of the **gradient** composition layer, are performed repeatedly to form a plurality of layers on top of the Si substrate, and generate a SiGe layer in which the **Ge** composition ratio varies with a series of steps inclined relative to the direction of the film growth.

Brief Summary Text - BSTX (18):

In contrast, in a method of forming a SiGe layer according to the present invention, because a step for epitaxially growing a SiGe **gradient** composition layer in which the **Ge** composition ratio gradually increases from the **Ge** composition ratio of the base material (Si in those cases where the base material for the growing process is a Si substrate, or SiGe in those cases where the base material is a constant composition layer), and a step for epitaxially growing a SiGe constant composition layer on top of the **gradient** composition layer in which the **Ge** composition ratio is the same as that of the final **Ge** composition ratio of the **gradient** composition layer are repeated a plurality of times, and furthermore because a semiconductor substrate of the present invention comprises a SiGe buffer layer constructed of a plurality of laminated layers comprising alternating **gradient** composition layers and constant composition layers, this buffer layer comprises a plurality of alternating **gradient** composition layers and constant composition layers with the **Ge** composition ratio in a series of inclined steps, and this state enables

a SiGe layer to be formed for which the dislocation density is low and the surface roughness is limited.

Brief Summary Text - BSTX (25):

Furthermore, in yet another method of forming a SiGe layer according to the present invention, it is also effective to gradually decrease the thickness of the gradient composition layer and the constant composition layer in the epitaxial growth steps after each step repetition. Namely, dislocation will nucleate more readily with higher **Ge** composition, and so if film formation is conducted with a single uniform thickness, then the uppermost layer will display greater dislocation density, whereas according to the method of the present invention, by gradually reducing the thickness of the **gradient** composition layer and the constant composition layer after each step repetition, a more equal distribution of dislocation can be achieved through each of the layers.

Brief Summary Text - BSTX (36):

According to a semiconductor substrate of the present invention, a SiGe buffer layer is provided which is constructed of a plurality of laminated layers comprising alternating **gradient** composition layers and constant composition layers, and according to a method of forming a SiGe layer of the present invention, a step for epitaxially growing a **gradient** composition layer and a step for epitaxially growing a constant composition layer are repeated a plurality of times, forming a SiGe layer in which the **Ge** composition ratio varies with a series of steps inclined relative to the direction of the film growth, and as a result, the occurrence of high densities of dislocations at the interfaces can be suppressed, and moreover dislocations are able to propagate in a lateral direction so as not to penetrate through to the surface.

Detailed Description Text - DETX (3):

FIG. 1 shows the cross-sectional structure of a semiconductor wafer (semiconductor substrate) WO and a semiconductor wafer with a strained Si layer (semiconductor substrate) W according to the present invention, and as follows is a description of the structure of these semiconductor wafers, together with a description of the associated manufacturing process. First, as shown in FIG. 1, a Si.sub.1-x Ge.sub.x stepped **gradient** layer (SiGe buffer layer) 2 in which the **Ge** composition ratio x varies from 0 to y (for example y=0.3) in a series of steps inclined relative to the direction of the film growth is grown epitaxially, using a low pressure CVD method, on the top of a Si substrate 1 which has been prepared by pulling using CZ methods. Film formation by this low pressure CVD method uses H.sub.2 as a carrier gas, and SiH.sub.4 and GeH.sub.4 as source gases.

Detailed Description Text - DETX (4):

Next, a relaxation layer 3 with a constant **Ge** composition ratio of Si.sub.1-y Ge.sub.y is grown epitaxially on top of the stepped **gradient** layer 2, thereby completing preparation of the semiconductor wafer WO. In addition, by then forming a strained Si layer 4 by epitaxially growing Si on top of a relaxation layer 3 with a Ge composition ratio z (in this first embodiment z=y) of Si.sub.1-z Ge.sub.z, the semiconductor wafer with a strained Si layer W of the present invention can be prepared. The film thickness of each of the layers are, for example, 1.5 .mu.m for the stepped gradient layer 2, 0.7 to 0.8 .mu.m for the relaxation layer 3, and 15 to 22 nm for the strained Si layer 4.

Detailed Description Text - DETX (5):

The film formation of the aforementioned stepped **gradient** layer 2 is carried out by repeating, a plurality of times, a step for epitaxially growing a SiGe **gradient** composition layer 2a in which the **Ge** composition ratio is gradually increased from the **Ge** composition ratio of the base material up to a predetermined value, and a step for epitaxially growing a SiGe constant composition layer 2b on top of the SiGe **gradient** composition layer 2a in which the **Ge** composition ratio is the same as that of the final **Ge** composition ratio of the **gradient** composition layer 2a, as shown in FIG. 2 and FIG. 3.

Detailed Description Text - DETX (6):

For example, in the present embodiment, the stepped gradient layer 2 is formed by performing four repetitions of the epitaxial growth steps for forming the gradient composition layer 2a and the constant composition layer 2b. In other words, if one step is considered to comprise the epitaxial growth of one **gradient** composition layer 2a and one constant composition layer 2b, then the first step will comprise growing a first **gradient** composition layer 2a, in which the **Ge** composition ratio is gradually varied from 0 to 0.075, on top of the Si substrate 1, and then forming a first constant composition layer 2b with a **Ge** composition ratio of 0.075 thereon. Subsequently, in a second step, a second **gradient** composition layer 2a, in which the **Ge** composition ratio is gradually varied from 0.075 to 0.15 is grown on top of the first constant composition layer 2b with a **Ge** composition ratio of 0.075, and a second constant composition layer 2b with a **Ge** composition ratio of 0.15 is then formed thereon.

Detailed Description Text - DETX (10):

In a semiconductor wafer W comprising a semiconductor wafer WO of the present embodiment and a strained Si layer, because a step for epitaxially growing a SiGe **gradient** composition layer 2a in which the **Ge** composition ratio

gradually increases from the **Ge** composition ratio of the base material (Si in those cases where the base for the growing process is the Si substrate 1, or SiGe in those cases where the base material is a constant composition layer 2b), and a step for epitaxially growing a SiGe constant composition layer 2b on top of the **gradient** composition layer 2a in which the **Ge** composition ratio is the same as that of the final **Ge** composition ratio of the **gradient** composition layer 2a are repeated a plurality of times, a layer is formed which comprises a plurality of alternating **gradient** composition layers 2a and constant composition layers 2b with the **Ge** composition ratio in a series of inclined steps, and as described above, this state enables the formation of a SiGe layer for which the dislocation density is low and the surface roughness is limited.

Claims Text - CLTX (7):

7. A method of forming a semiconductor substrate structure according to claim 1, comprising epitaxially growing on a substrate a SiGe **gradient** composition layer in which a **Ge** composition ratio increases gradually from a **Ge** composition ratio of a base material, and epitaxially growing on top of said **gradient** composition layer a SiGe constant composition layer in which a **Ge** composition ratio is equal to that of a final **Ge** composition ratio of said **gradient** composition layer, forming a plurality of layers on top of said Si substrate to generate a SiGe layer in which a **Ge** composition ratio varies with a series of steps inclined relative to a direction of film formation.